

A next-generation scalable video-processor core

Fall Processor Forum

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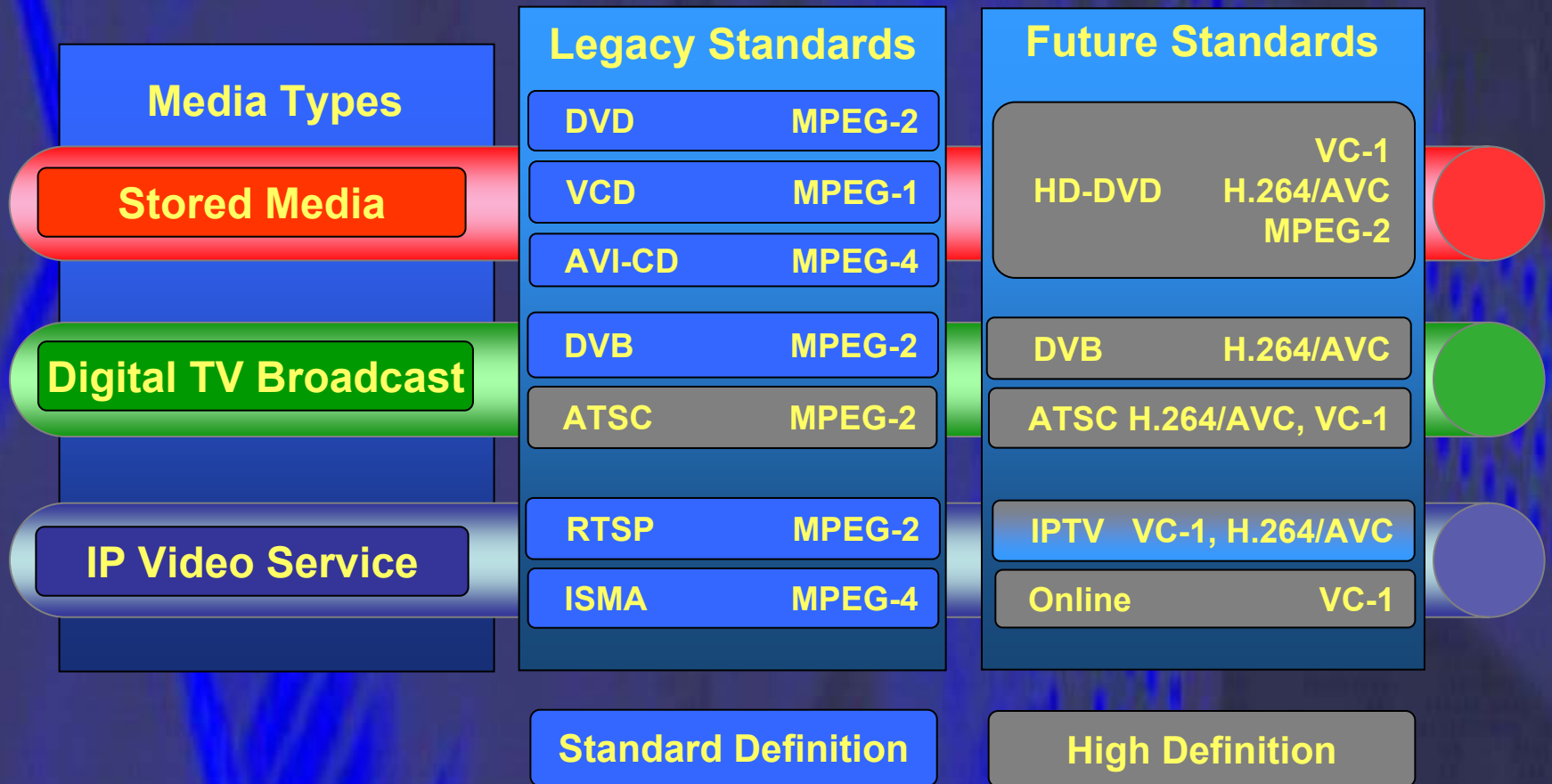
Outline

- **Multi-standard digital video**
- **The v-MP2 next-generation scalable video core**
- **Mobile video solution v-MP2000 M**
- **HDTV video solution v-MP2000 HD**
- **Conclusion**

Mobile & home multimedia

- **Mobile multimedia**
 - Multimedia phones
 - Mobile TV
 - Wireless PDAs
 - Portable video player (PVP)
- **Home multimedia**
 - HD-capable DTV & set-top boxes
 - HD-DVD
 - IPTV
 - Media centers
- **Convergence of mobile & home video applications**
 - New breed of consumer devices emerging
 - Common video standards as basis

Multi-standard digital video

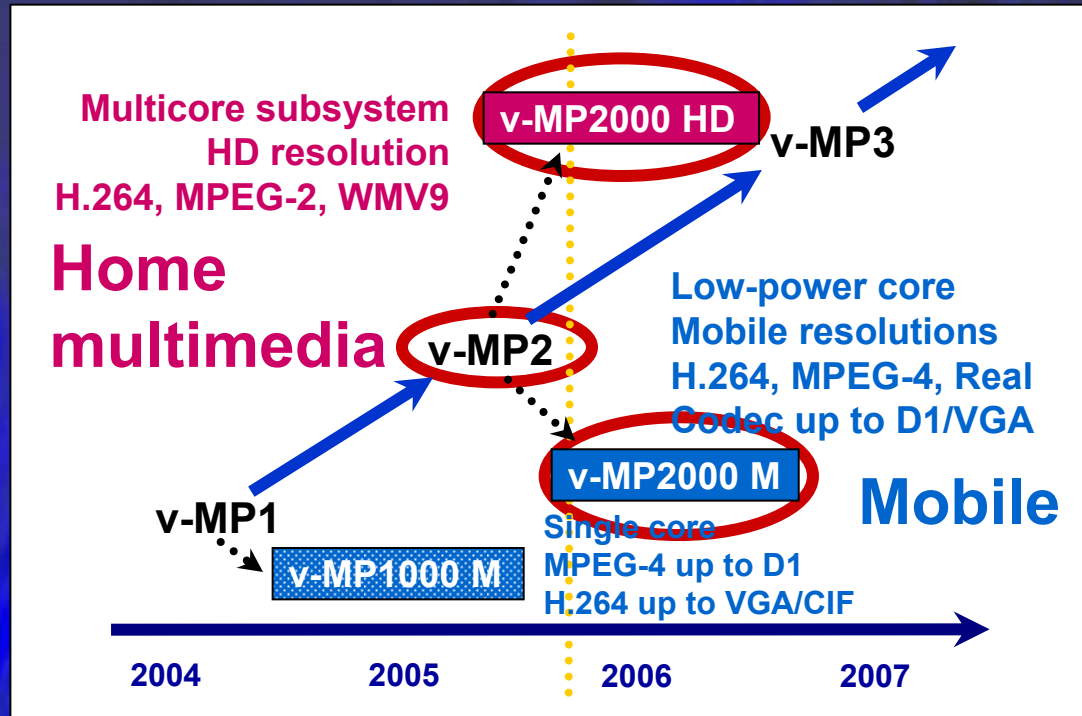


Flexibility demands on video solution

- **Programmability** for wide range of standards
- **Scalability** for wide range of formats



v-MPx product roadmap



- Common architecture roadmap
 - Evolution of scalable cores based on common architecture
 - Reuse application software for mobile and home segments
- Next-generation **mobile** solution: v-MP2000 M
- Next-generation **HDTV** solution: v-MP2000 HD

Multi-standard video decoding

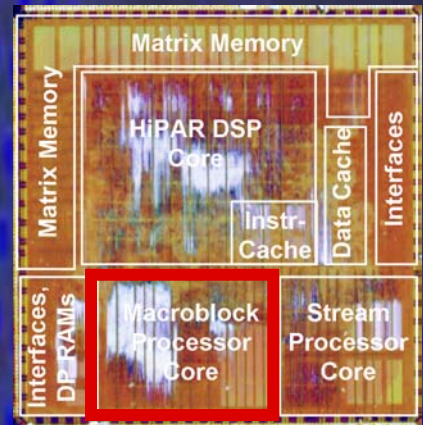
- Most relevant standards, home multimedia
 - H.264/AVC Main / High Profile
 - Microsoft VC-1 / WMV9
 - MPEG-4 ASP / DivX
 - MPEG-2
- Comparison of video standards (selected tools):

Tool	H.264	VC-1	MPEG-4 ASP	MPEG-2
Intra-prediction modes	13	2	2	
Motion-vector precision	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{4}$	$\frac{1}{2}$
Macro-block partitions in motion compensation	7	2	2	1
Global motion compensation			✓	
Loop filter	✓	✓		

- H.264 is the most demanding

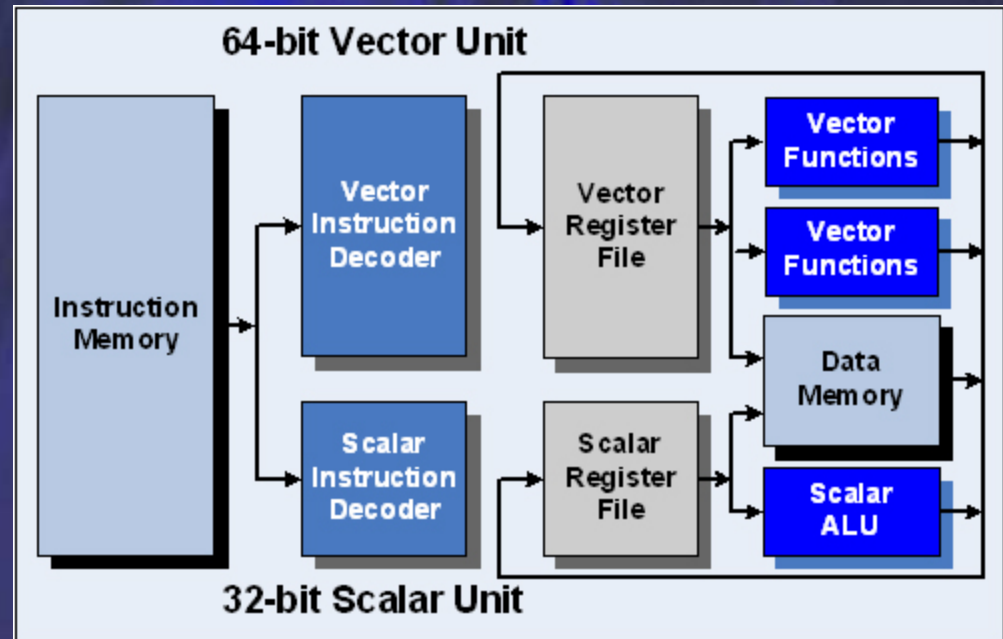
videantis next-generation v-MP2 core

- Successor of the silicon-proven v-MP1
- v-MP1 capabilities:
 - 200MHz @ 0.13 μ technology
 - H.264 baseline decoding VGA @ 30fps
- Design goal for v-MP2
 - 2x application-specific performance improvement
 - Built-in scalability on two levels:
 - Single-core scalability
 - Multicore scalability
 - Targeting both mobile & home multimedia



v-MP2 scalable architecture template

- **Dual-issue VLIW core**
 - Vector unit (64 Bit, splittable)
 - Scalar unit (32 Bit)
- **Execution unit scalability**
 - Up to twice as many execution units as v-MP1
- **ISA extensions scalability**
- **Configurable memory sizes**
 - Vector register file: 32 to 64 registers
 - Instruction memory: 16KB to 32KB
 - Data memory: 4KB to 8KB
- **Single- and multi-channel DMA**



Design of ISA extensions

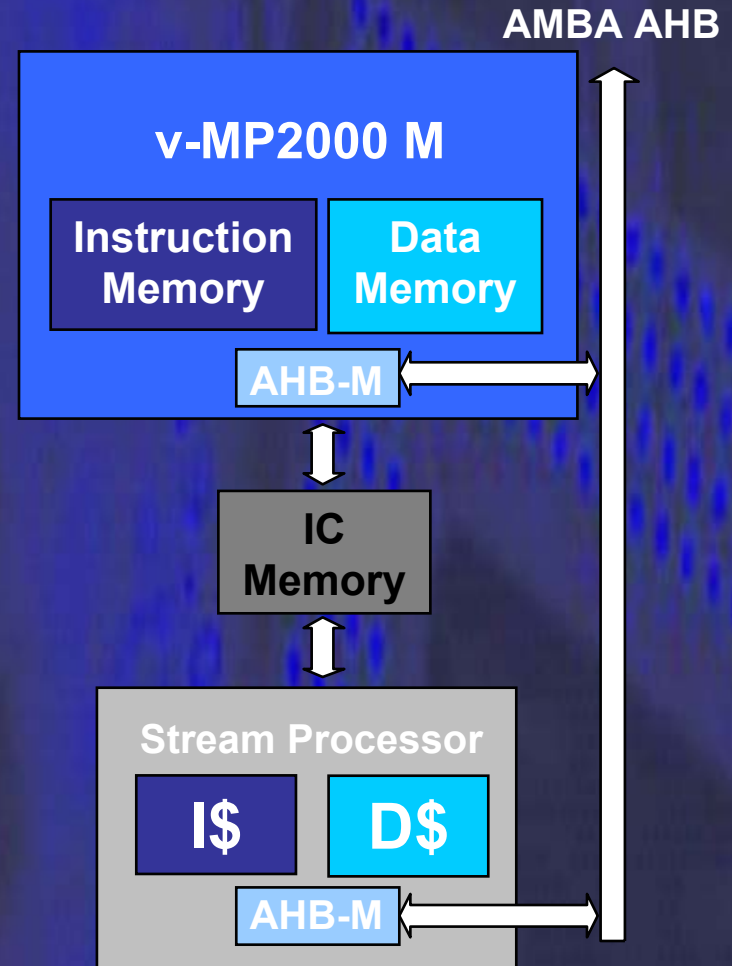
- **Set of instructions adapted towards video schemes**
 - Fully integrated into datapath and pipeline scheme
 - No dedicated, inflexible accelerator blocks
 - Functions general enough to support multiple schemes
- **Design of adapted ISA extensions**
 - Requires deep domain-specific knowledge
 - Hand-crafted by videantis, based on existing software implementations and algorithm analysis
- **Continuing definition of future ISA extensions**
 - Based on input, e.g., from ongoing standardization activities
 - Advancing the v-MPx roadmap

ISA extensions scalability

- Selection of ISA extensions depends on target application field
 - Involves performance / area trade-off
- Optimal choice is the expertise of videantis
 - Fully tailored solution; no customer intervention required
- Predefined solution packages for
 - Mobile multimedia
 - Lowest power, smallest footprint
 - H.264, MPEG-4, Real codec up to D1/VGA
 - Home multimedia
 - Highest performance
 - H.264, WMV9, MPEG-2 1080i decoding
 - Solution packages include optimized software implementations

Mobile video solution: v-MP2000 M

- Multimedia functionality provided by v-MP2000 M
 - H.264 baseline profile decoding up to D1 @ 200MHz
- Stream processor for bitstream processing
 - ARM, MIPS, custom core
- Data exchange via intercore memory
 - Generic interface, supports all standards
- 32/64-bit AMBA AHB bus for system integration

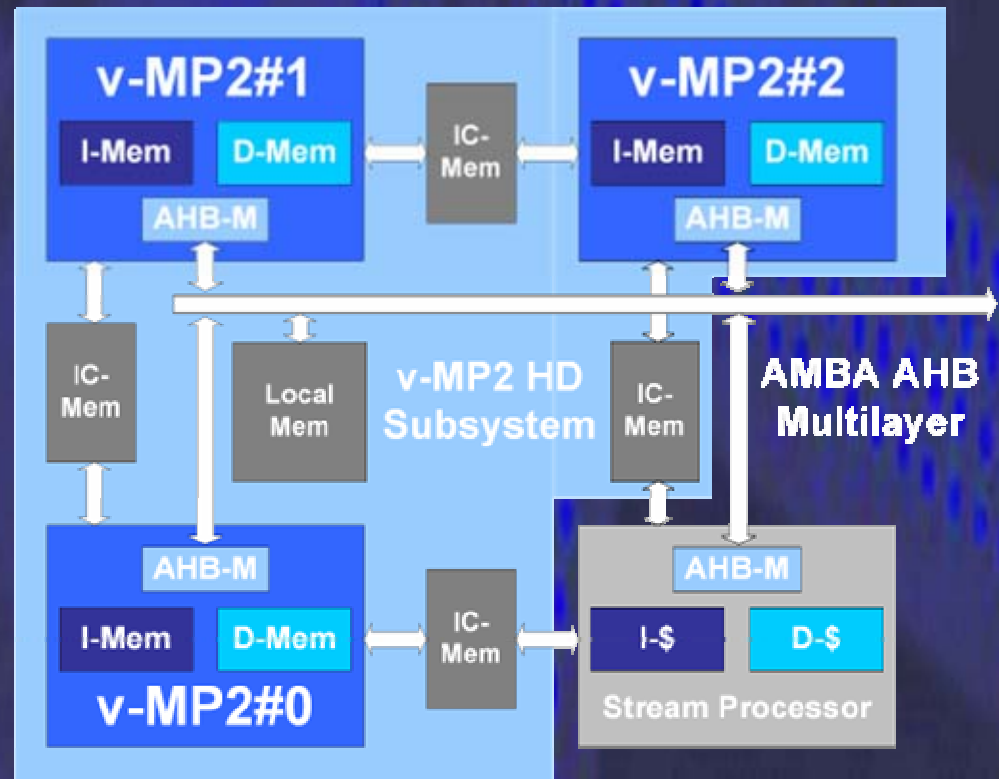


v-MP2000 M implementation data

- **Fully synthesizable core**
 - 120k gates core logic
 - Register files: 2R/1W, 4R/2W
 - SRAMs: I-mem 1R/1W, D-mem 2R/2W, intercore mem 2R/2W
- **Very small overall silicon area**
 - 2.61mm² *including* memories in a 0.13μ process
- **Very low power consumption**
 - 90mW @ 200MHz
- **Fully optimized software applications suite**
 - Support for all relevant standards
 - Custom enhancements for vendor-specific extensions
 - Pre-/postprocessing, frame rate conversion, image enhancements, ...

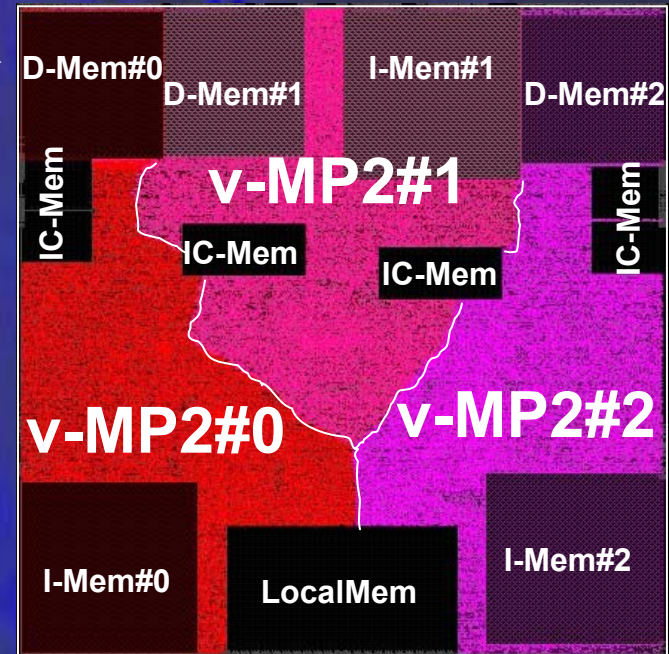
HDTV video solution v-MP2000 HD

- v-MP2000 HD system architecture based on v-MP2 core
 - H.264, MPEG-2, WMV9 1080i decoding
- Video subsystem
 - 3 v-MP2 cores
 - Intercore memories
 - On-chip scratch pad memory
 - AMBA multilayer
- Stream processor
 - videantis v-SP2 or custom core



v-MP2000 HD implementation data

- Video subsystem floorplan
- Clock speed target: 300MHz
- Total gate count / area estimates for 0.13 μ technology
 - 450k gates core logic for 3 cores
 - 11mm² silicon area including memories
- FPGA-verified prototype
 - Evaluation of task partitioning scheme and performance
- Multicore application performance
 - H.264 high profile 1080i decoding @ 300MHz



Multicore task partitioning

- Principle: Macro-pipelining of tasks
- Flexible task assignment to cores
 - Code modules reloadable in the background
- Example: H.264 task assignment
 - Depending on slice type

Core	I-Slice	P-Slice	B-Slice
MP#0	Integer transform Intra prediction	Integer transform	Integer transform Inter prediction
MP#1	Loop filter	Inter prediction	Inter prediction
MP#2	Loop filter	Loop filter	Loop filter

Conclusion

- **Multi-standard, multi-format video requires programmability and scalability**
 - Targeting mobile & home multimedia
- **Next-generation v-MP2 core**
 - 2x application performance
 - Built-in scalability on single- & multicore level
- **Single-core mobile solution: v-MP2000 M**
 - Next generation high-quality video communication & mobile TV
- **Multicore HD solution: v-MP2000 HD**
 - Highest-quality digital TV and set-top boxes